

LM833-N Dual Audio Operational Amplifier

Check for Samples: [LM833-N](#)

FEATURES

- **Wide Dynamic Range:** >140dB
- **Low Input Noise Voltage:** $4.5\text{nV}/\sqrt{\text{Hz}}$
- **High Slew Rate:** $7\text{ V}/\mu\text{s}$ (typ); $5\text{ V}/\mu\text{s}$ (Min)
- **High Gain Bandwidth:** 15MHz (typ); 10MHz (Min)
- **Wide Power Bandwidth:** 120KHz
- **Low Distortion:** 0.002%
- **Low Offset Voltage:** 0.3mV
- **Large Phase Margin:** 60°
- **Available in 8 Pin VSSOP Package**

DESCRIPTION

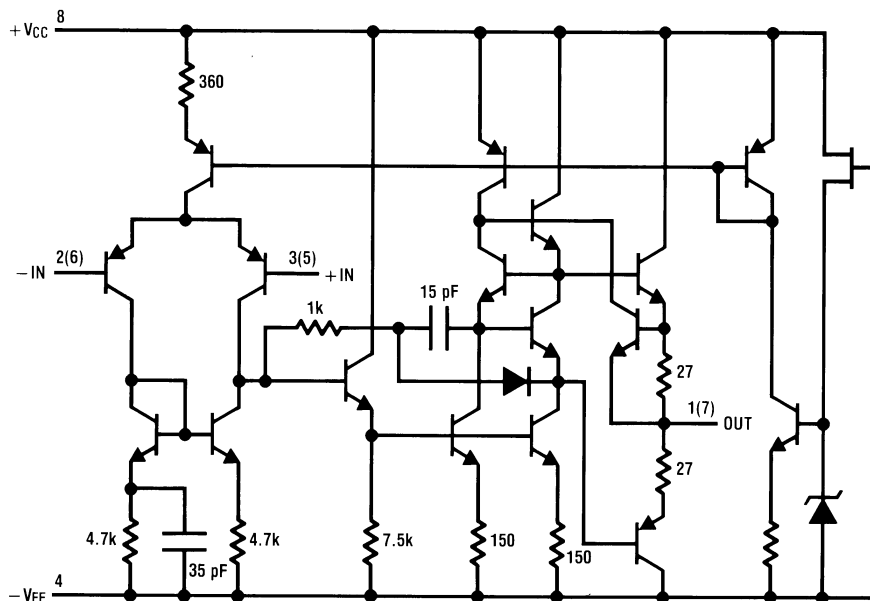
The LM833-N is a dual general purpose operational amplifier designed with particular emphasis on performance in audio systems.

This dual amplifier IC utilizes new circuit and processing techniques to deliver low noise, high speed and wide bandwidth without increasing external components or decreasing stability. The LM833-N is internally compensated for all closed loop gains and is therefore optimized for all preamp and high level stages in PCM and HiFi systems.

The LM833-N is pin-for-pin compatible with industry standard dual operational amplifiers.

Schematic Diagram

(1/2 LM833-N)



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Connection Diagram

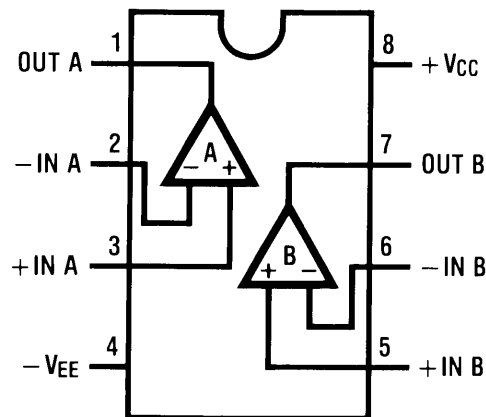


Figure 1. See Package Number D0008A, P0008E or DGK0008A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Supply Voltage $V_{CC}-V_{EE}$		36V	
Differential Input Voltage ⁽³⁾ V_I		$\pm 30V$	
Input Voltage Range ⁽³⁾ V_{IC}		$\pm 15V$	
Power Dissipation ⁽⁴⁾ P_D		500 mW	
Operating Temperature Range T_{OPR}		$-40 \sim 85^\circ C$	
Storage Temperature Range T_{STG}		$-60 \sim 150^\circ C$	
Soldering Information	PDIP Package	Soldering (10 seconds)	260°C
	Small Outline Package (SOIC and VSSOP)	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C
ESD tolerance ⁽⁵⁾		1600V	

- (1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) If supply voltage is less than $\pm 15V$, it is equal to supply voltage.
- (4) This is the permissible value at $T_A \leq 85^\circ C$.
- (5) Human body model, 1.5 k Ω in series with 100 pF.

DC ELECTRICAL CHARACTERISTICS⁽¹⁾⁽²⁾

 $(T_A = 25^\circ\text{C}, V_S = \pm 15\text{V})$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$R_S = 10\Omega$		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Voltage Gain	$R_L = 2\text{ k}\Omega, V_O = \pm 10\text{V}$	90	110		dB
V_{OM}	Output Voltage Swing	$R_L = 10\text{ k}\Omega$	± 12	± 13.5		V
		$R_L = 2\text{ k}\Omega$	± 12	± 13.4		V
V_{CM}	Input Common-Mode Range		± 12	± 14.0		V
CMRR	Common-Mode Rejection Ratio	$V_{IN} = \pm 12\text{V}$	80	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = 15 \sim 5\text{V}, -15 \sim -5\text{V}$	80	100		dB
I_Q	Supply Current	$V_O = 0\text{V}$, Both Amps		5	8	mA

- (1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (2) All voltages are measured with respect to the ground pin, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS

 $(T_A = 25^\circ\text{C}, V_S = \pm 15\text{V}, R_L = 2\text{ k}\Omega)$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR	Slew Rate	$R_L = 2\text{ k}\Omega$	5	7		V/ μs
GBW	Gain Bandwidth Product	$f = 100\text{ kHz}$	10	15		MHz
V_{NI}	Equivalent Input Noise Voltage (LM833AM, LM833AMX)	RIAA, $R_S = 2.2\text{ k}\Omega$ ⁽¹⁾			1.4	μV

- (1) RIAA Noise Voltage Measurement Circuit

DESIGN ELECTRICAL CHARACTERISTICS

 $(T_A = 25^\circ\text{C}, V_S = \pm 15\text{V})$

The following parameters are not tested or ensured.

Symbol	Parameter	Conditions	Typ	Units
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage		2	$\mu\text{V}/^\circ\text{C}$
THD	Distortion	$R_L = 2\text{ k}\Omega, f = 20\sim 20\text{ kHz}$ $V_{OUT} = 3\text{ V}_{rms}, A_V = 1$	0.002	%
e_n	Input Referred Noise Voltage	$R_S = 100\Omega, f = 1\text{ kHz}$	4.5	$\text{nV} / \sqrt{\text{Hz}}$
i_n	Input Referred Noise Current	$f = 1\text{ kHz}$	0.7	$\text{pA} / \sqrt{\text{Hz}}$
PBW	Power Bandwidth	$V_O = 27\text{ V}_{pp}, R_L = 2\text{ k}\Omega, \text{THD} \leq 1\%$	120	kHz
f_U	Unity Gain Frequency	Open Loop	9	MHz
Φ_M	Phase Margin	Open Loop	60	deg
	Input Referred Cross Talk	$f = 20\sim 20\text{ kHz}$	-120	dB

TYPICAL PERFORMANCE CHARACTERISTICS

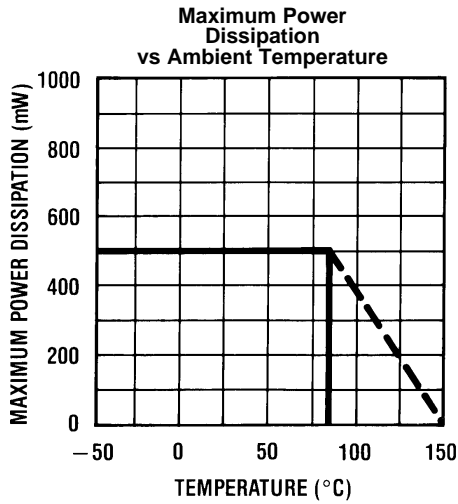


Figure 2.

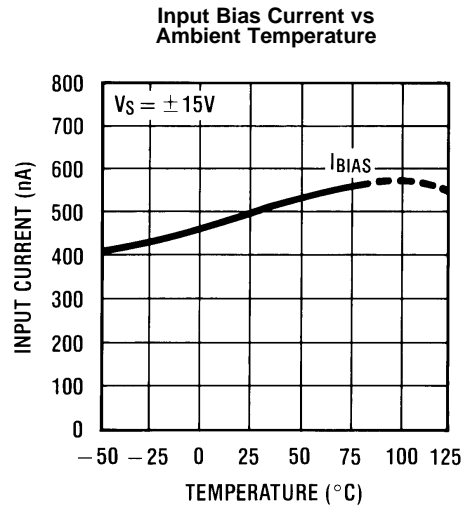


Figure 3.

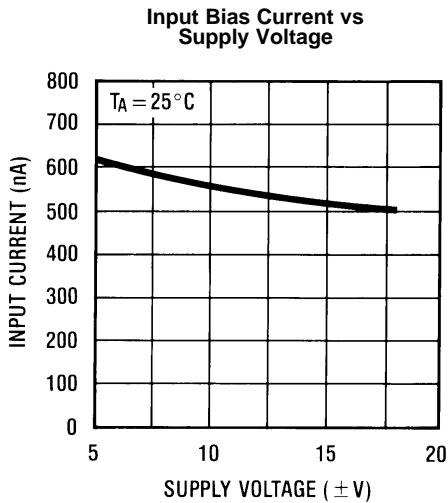


Figure 4.

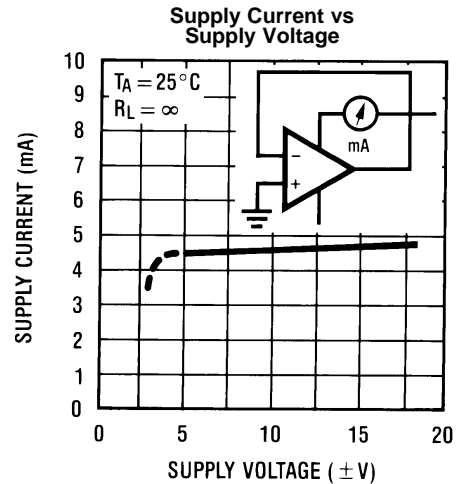


Figure 5.

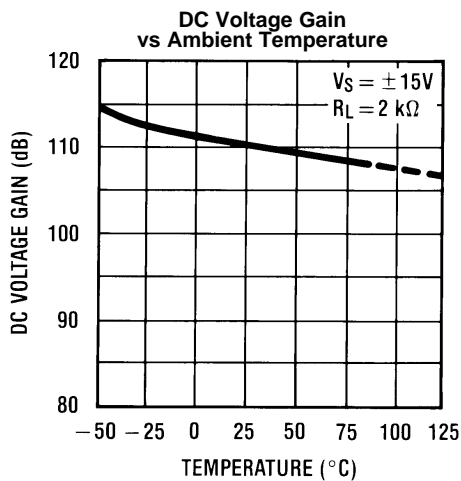


Figure 6.

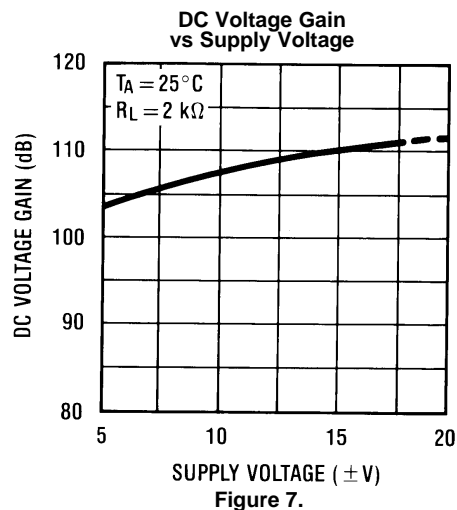
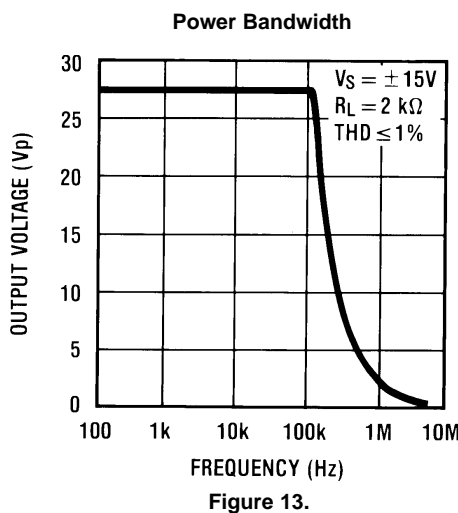
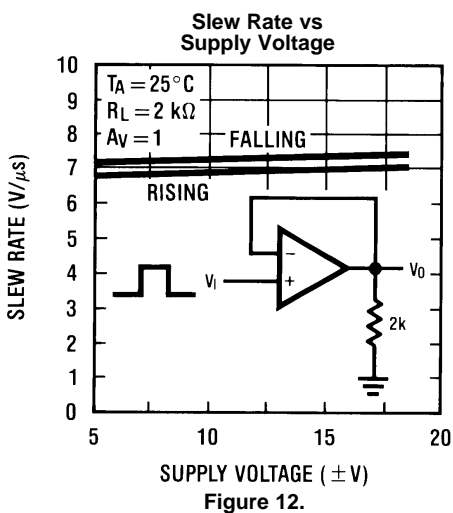
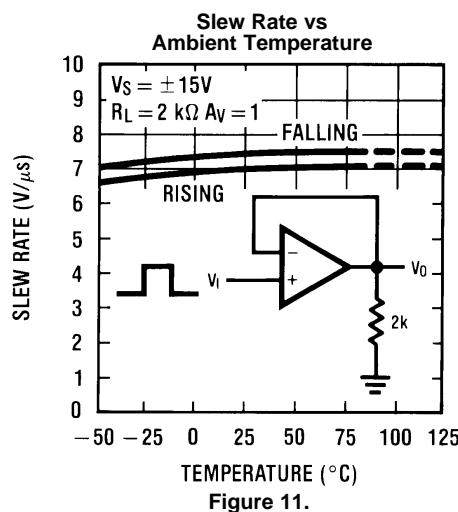
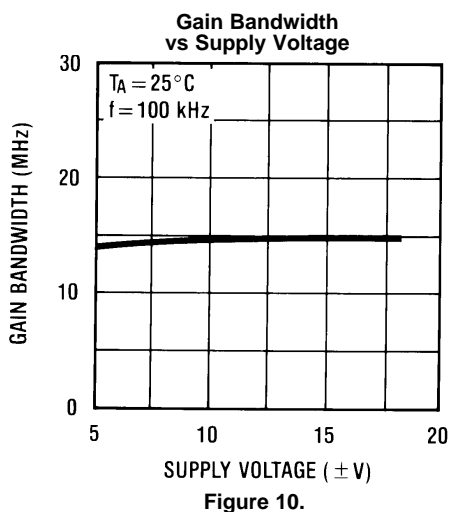
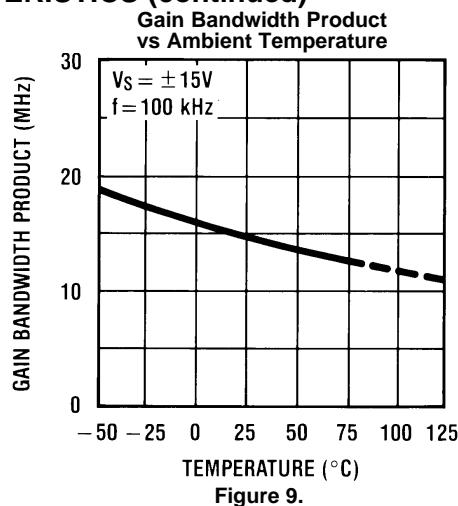
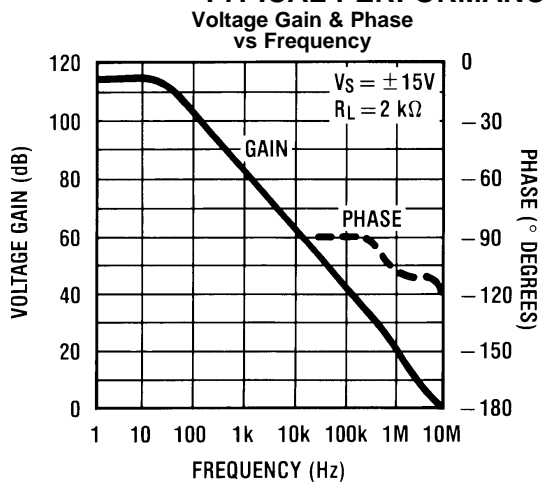
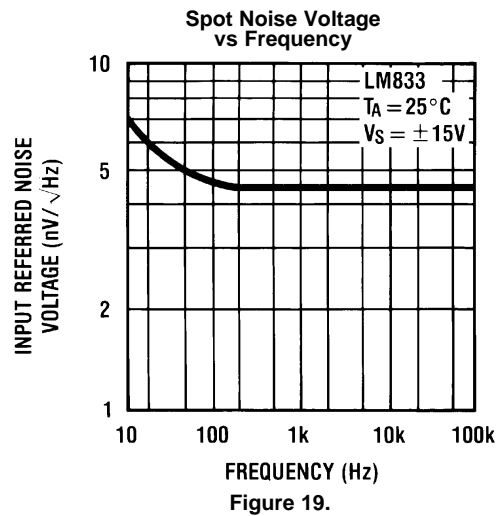
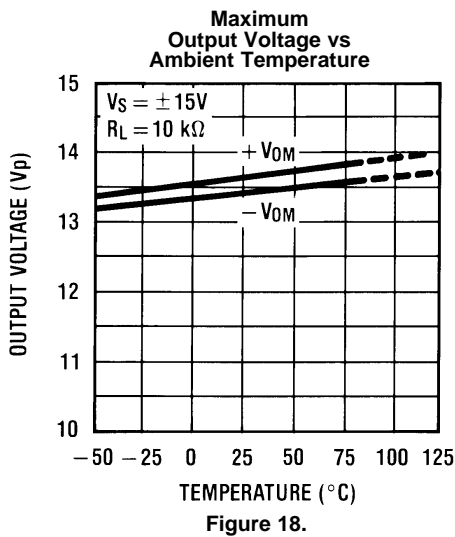
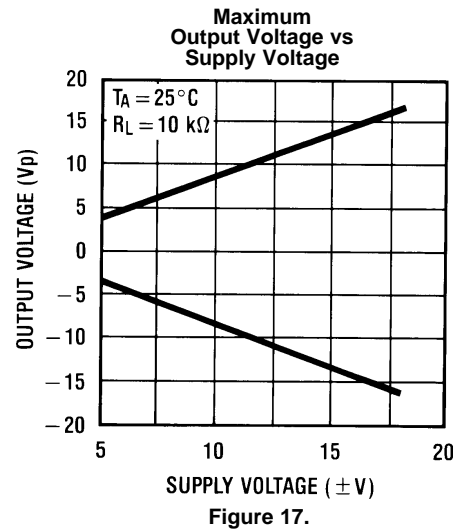
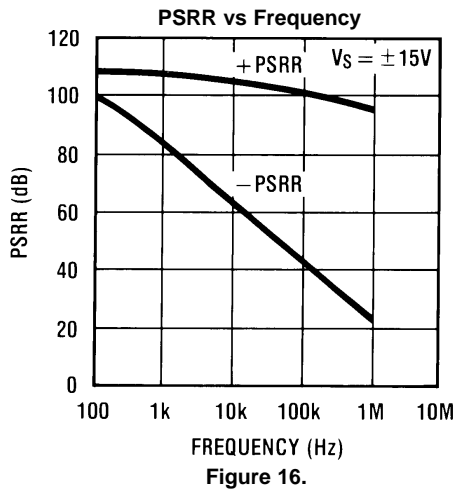
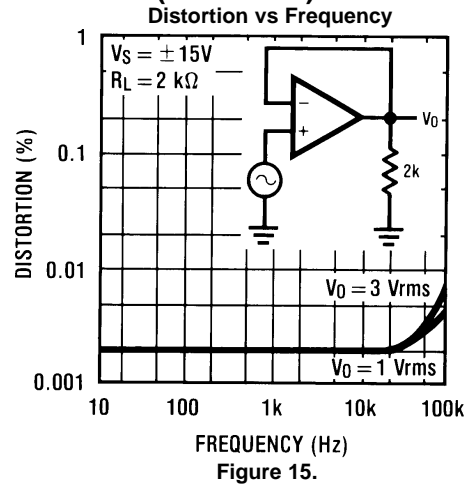
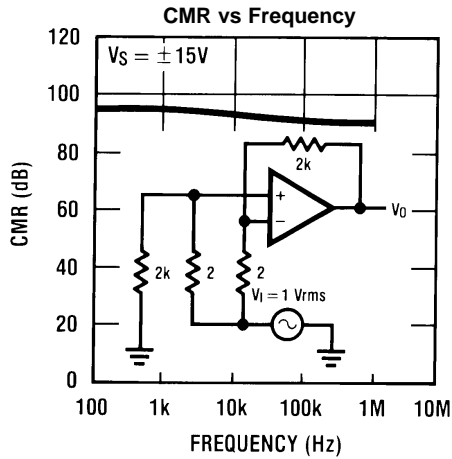


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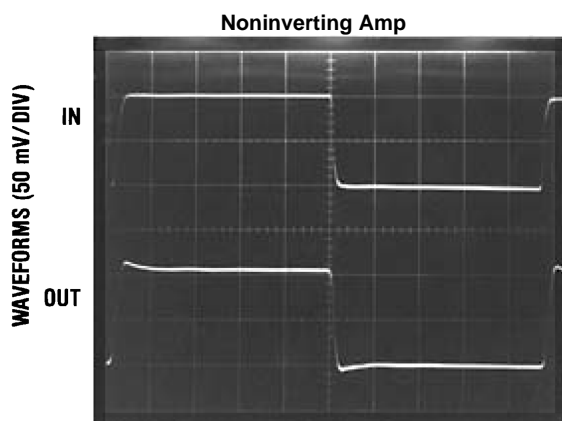
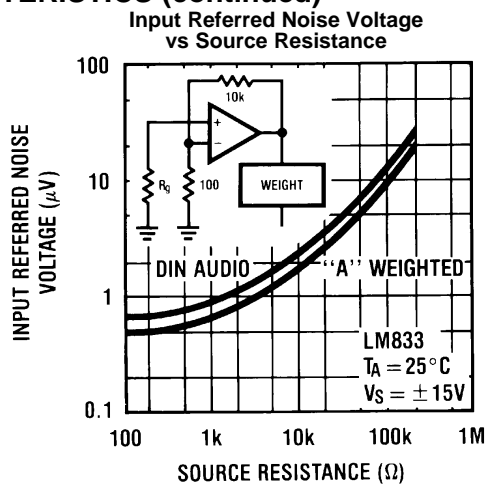
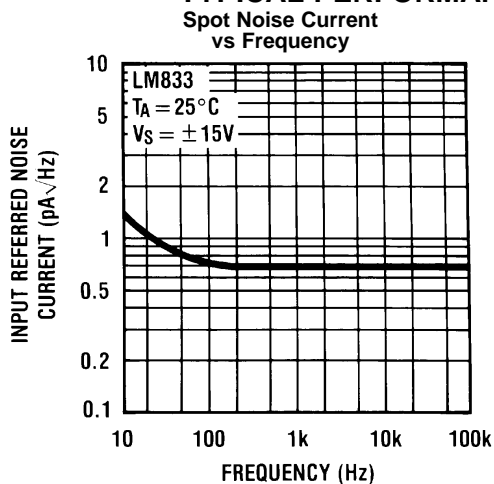
TYPICAL PERFORMANCE CHARACTERISTICS (continued)



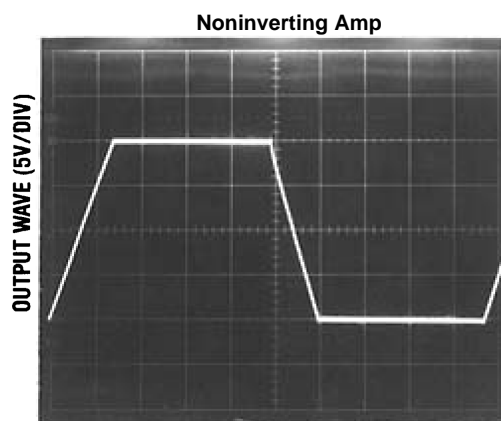
TYPICAL PERFORMANCE CHARACTERISTICS (continued)



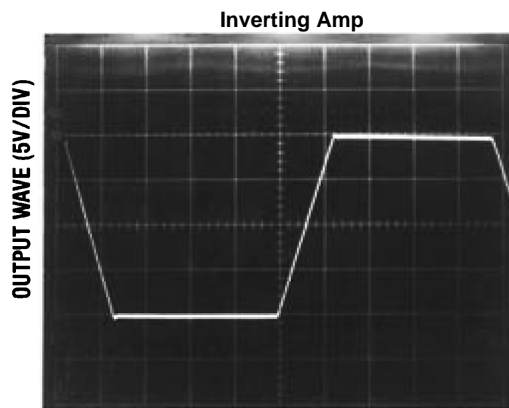
TYPICAL PERFORMANCE CHARACTERISTICS (continued)



TIME (0.2 μs/DIV)



TIME (2 μs/DIV)



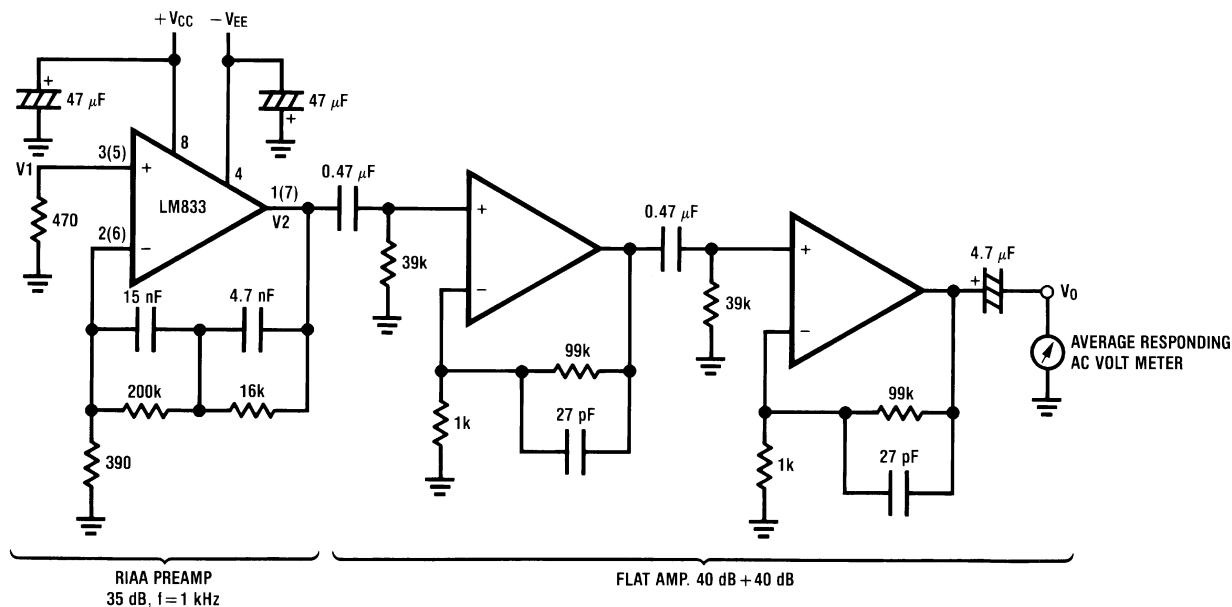
TIME (2 μs/DIV)

APPLICATION HINTS

The LM833-N is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 50 pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 50 pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

Noise Measurement Circuit



Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.

**Figure 25. Total Gain: 115 dB @f = 1 kHz
Input Referred Noise Voltage: $e_n = V_0/560,000$ (V)**

RIAA Noise Voltage Measurement Circuit

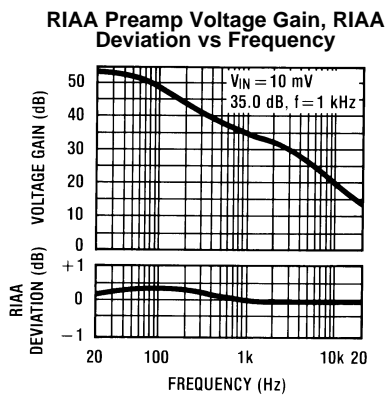
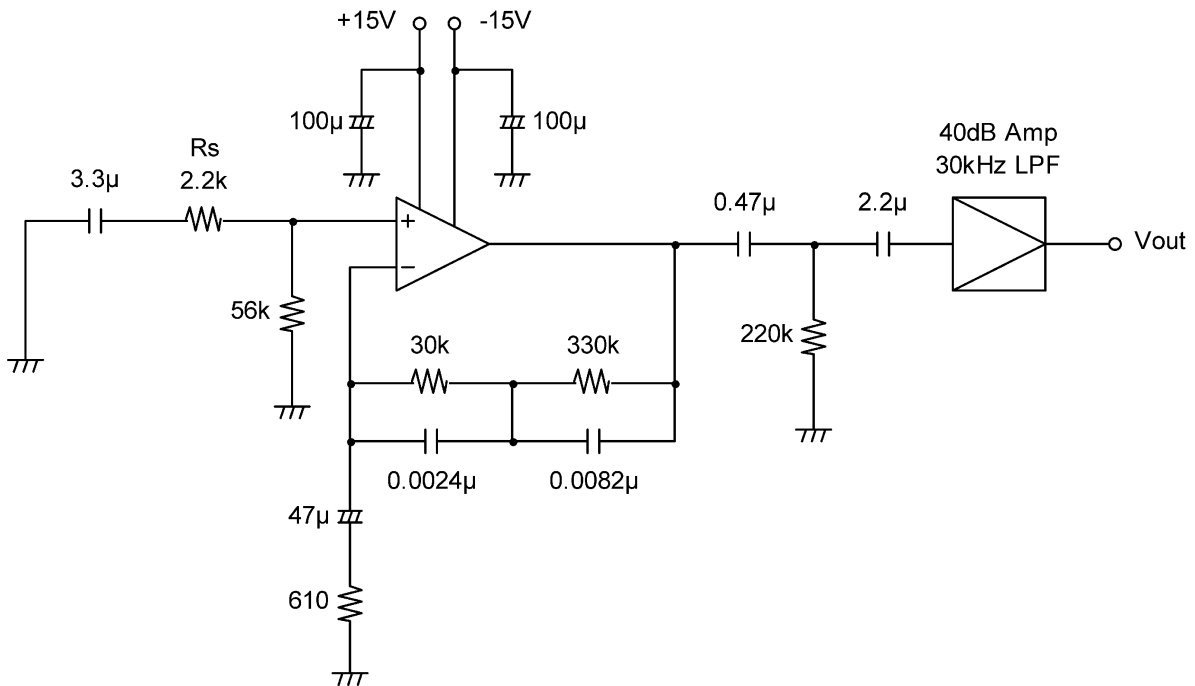


Figure 26.

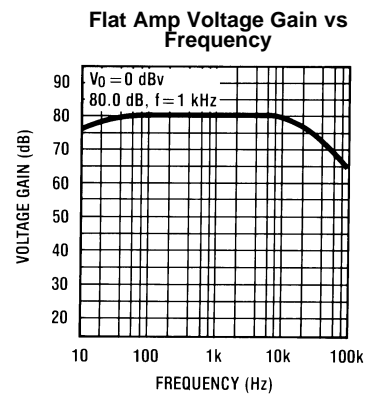
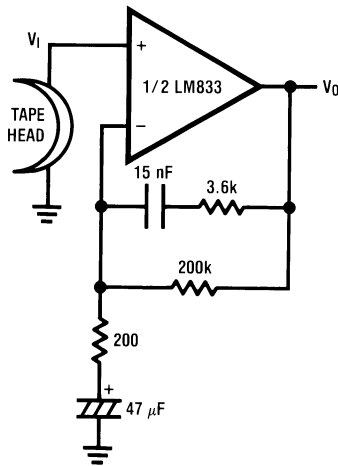


Figure 27.

Typical Applications



$A_V = 34.5$
 $F = 1 \text{ kHz}$
 $E_n = 0.38 \mu\text{V}$
 A Weighted

Figure 28. NAB Preamp

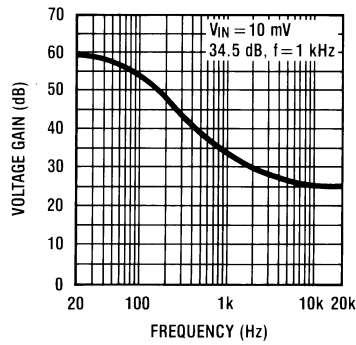
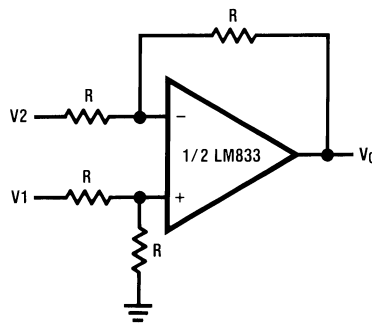
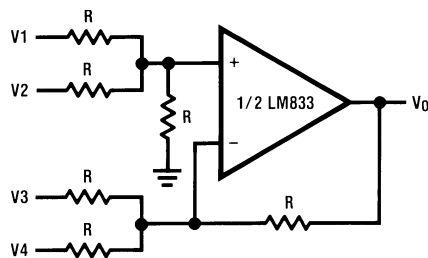


Figure 29. NAB Preamp Voltage Gain vs Frequency



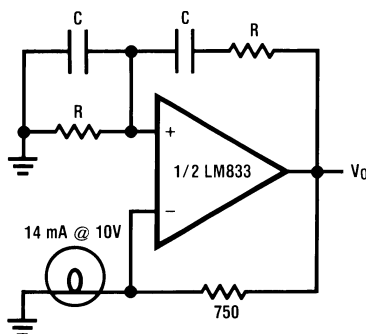
$V_O = V1 - V2$

Figure 30. Balanced to Single Ended Converter



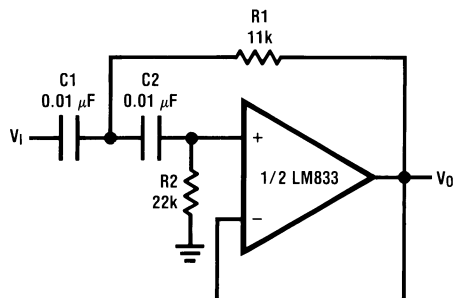
$$V_O = V_1 + V_2 - V_3 - V_4$$

Figure 31. Adder/Subtracter



$$f_o = \frac{1}{2\pi RC}$$

Figure 32. Sine Wave Oscillator



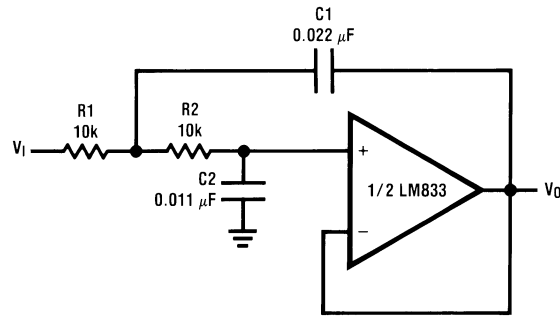
if $C_1 = C_2 = C$

$$R_1 = \frac{\sqrt{2}}{2\omega_0 C}$$

$$R_2 = 2 \cdot R_1$$

Illustration is $f_0 = 1 \text{ kHz}$

Figure 33. Second Order High Pass Filter (Butterworth)



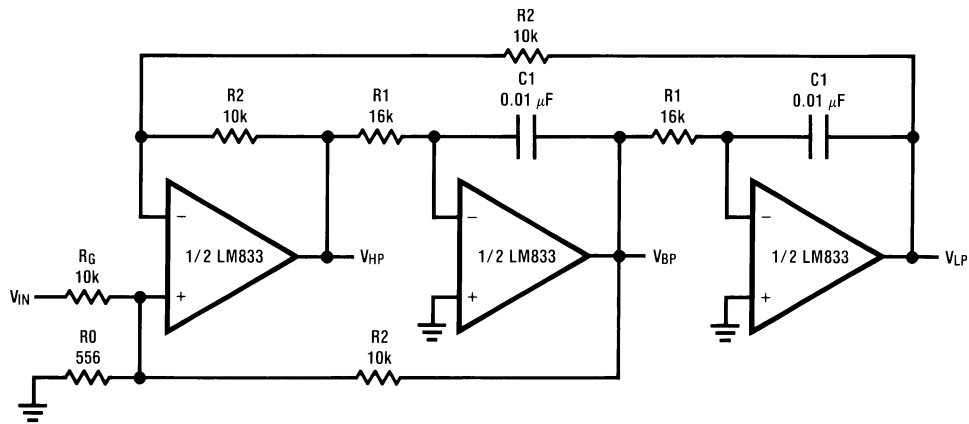
if $R1 = R2 = R$

$$C1 = \frac{\sqrt{2}}{\omega_0 R}$$

$$C2 = \frac{C1}{2}$$

Illustration is $f_0 = 1 \text{ kHz}$

Figure 34. Second Order Low Pass Filter (Butterworth)



$$f_0 = \frac{1}{2\pi C1 R1}, Q = \frac{1}{2} \left(1 + \frac{R2}{R0} + \frac{R2}{RG} \right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$$

Illustration is $f_0 = 1 \text{ kHz}, Q = 10, A_{BP} = 1$

Figure 35. State Variable Filter

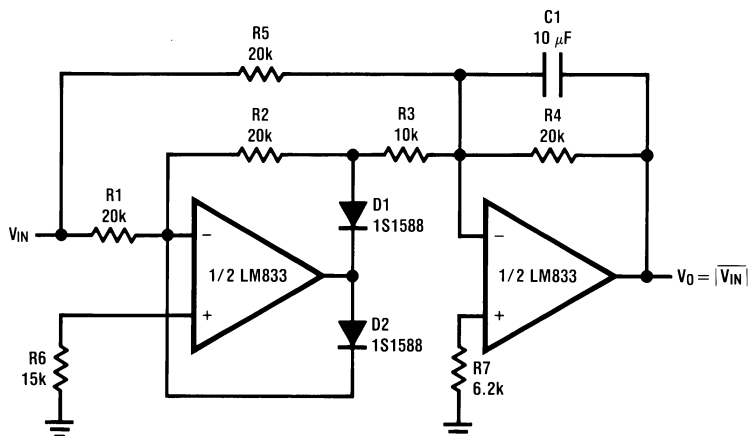


Figure 36. AC/DC Converter

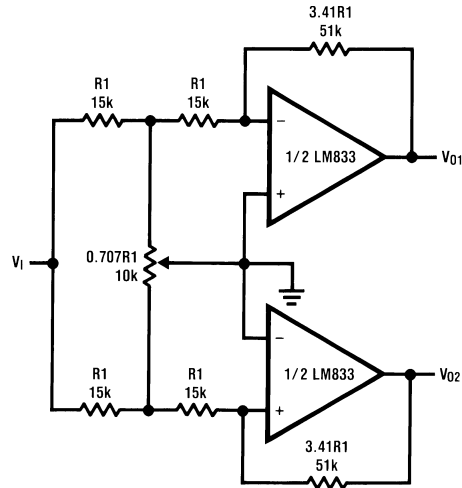


Figure 37. 2 Channel Panning Circuit (Pan Pot)

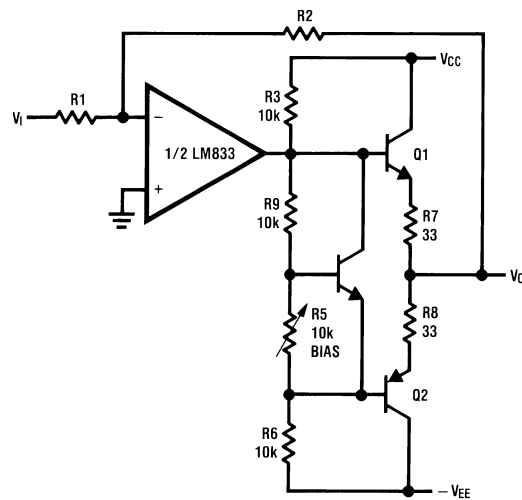
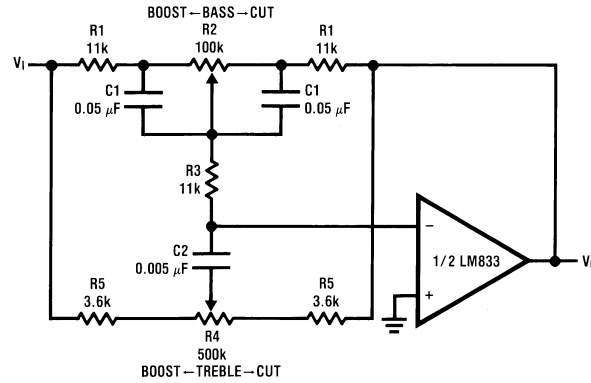


Figure 38. Line Driver



$$f_L = \frac{1}{2\pi R_2 C_1}, f_{LB} = \frac{1}{2\pi R_1 C_1}$$

$$f_H = \frac{1}{2\pi R_5 C_2}, f_{HB} = \frac{1}{2\pi (R_1 + R_5 + 2R_3) C_2}$$

Illustration is:

$f_L = 32 \text{ Hz}$, $f_{LB} = 320 \text{ Hz}$
 $f_H = 11 \text{ kHz}$, $f_{HB} = 1.1 \text{ kHz}$

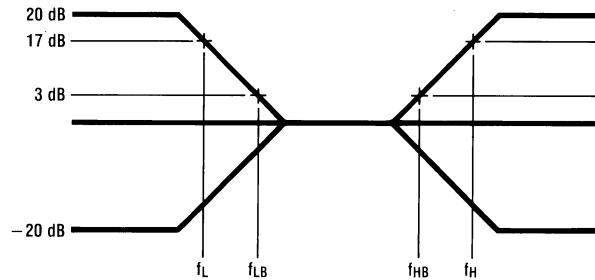
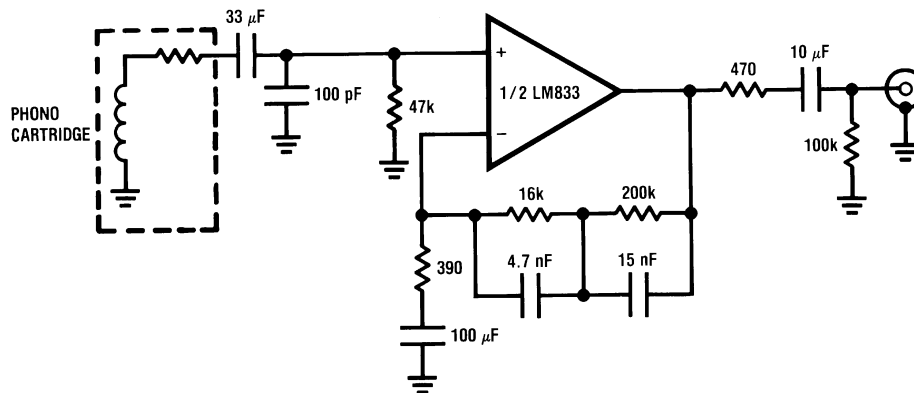
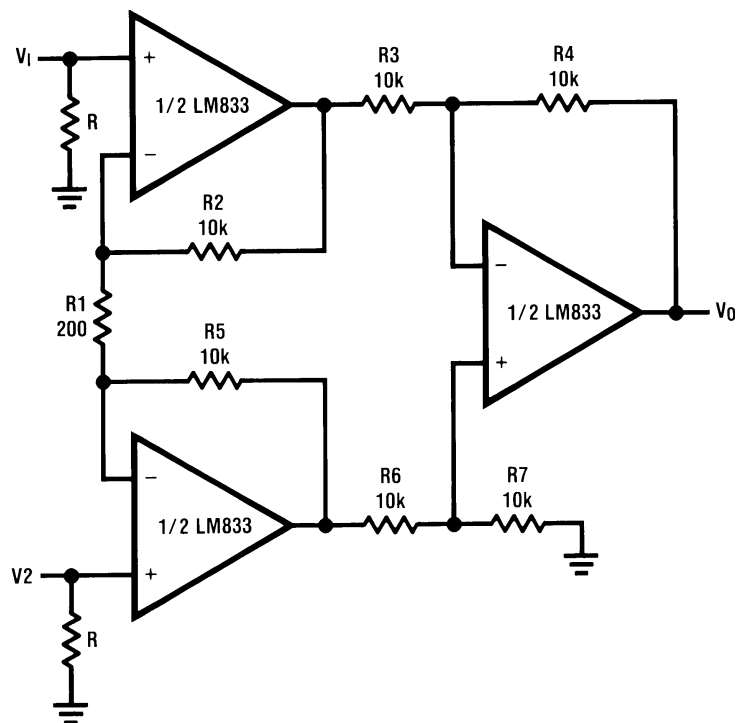


Figure 39. Tone Control



$A_v = 35 \text{ dB}$
 $E_n = 0.33 \mu\text{V}$
 $S/N = 90 \text{ dB}$
 $f = 1 \text{ kHz}$
 A Weighted
 A Weighted, $V_{IN} = 10 \text{ mV}$
 @ $f = 1 \text{ kHz}$

Figure 40. RIAA Preamp



If $R_2 = R_5$, $R_3 = R_6$, $R_4 = R_7$

$$V_0 = \left(1 + \frac{2R_2}{R_1}\right) \frac{R_4}{R_3} (V_2 - V_1)$$

Illustration is:
 $V_0 = 101(V_2 - V_1)$

Figure 41. Balanced Input Mic Amp

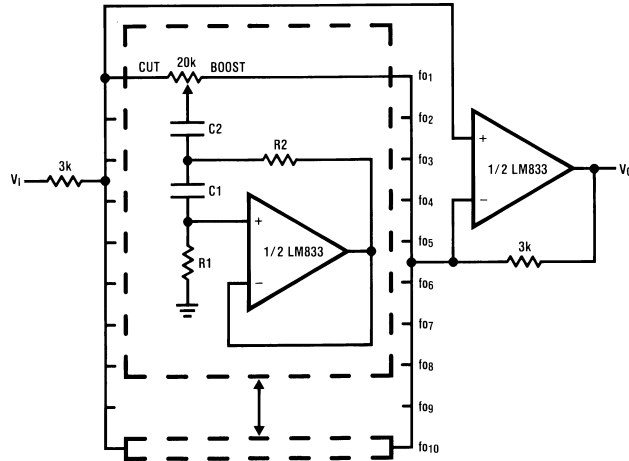


Figure 42. 10 Band Graphic Equalizer

fo (Hz)	C ₁	C ₂	R ₁	R ₂
32	0.12μF	4.7μF	75kΩ	500Ω
64	0.056μF	3.3μF	68kΩ	510Ω
125	0.033μF	1.5μF	62kΩ	510Ω
250	0.015μF	0.82μF	68kΩ	470Ω
500	8200pF	0.39μF	62kΩ	470Ω
1k	3900pF	0.22μF	68kΩ	470Ω
2k	2000pF	0.1μF	68kΩ	470Ω
4k	1100pF	0.056μF	62kΩ	470Ω
8k	510pF	0.022μF	68kΩ	510Ω
16k	330pF	0.012μF	51kΩ	510Ω

Note: At volume of change = ±12 dB Q = 1.

LM833-N MDC MWC DUAL AUDIO OPERATIONAL AMPLIFIER

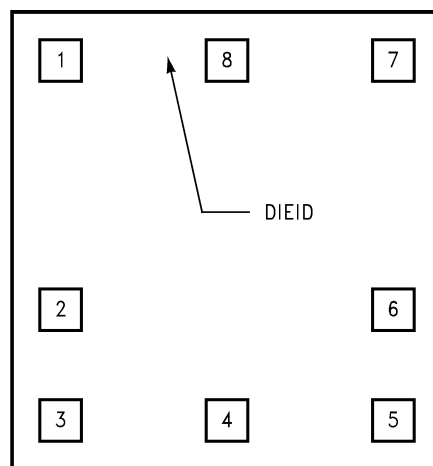


Figure 43. Die Layout (A - Step)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM833M	ACTIVE	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LM833 M	Samples
LM833M/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM833 M	Samples
LM833MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	Z83	Samples
LM833MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	Z83	Samples
LM833MX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM833 M	Samples
LM833N/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM 833N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM833MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM833MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM833MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM833MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM833MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM833MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM833M	D	SOIC	8	95	495	8	4064	3.05
LM833M	D	SOIC	8	95	495	8	4064	3.05
LM833M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM833N/NOPB	P	PDIP	8	40	502	14	11938	4.32



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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